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Code No.: 9A04605/R09

B.Tech. III Year II Semester Regular & Supplementary Examinations **Set-4**

April/May - 2013

VLSI DESIGN

(Common to ECE, EIE and E.Con.E)

Time: 3 Hours Max. Marks: 70

*Answer any **FIVE** Questions*

***All** Questions carry **equal** marks*

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1. (a) Explain the evaluation of a VLSI design technology.
   (b) Explain clearly about Moore's law.)

2. (a) Draw the circuit of nMOS inverter and explain its operation. Draw and explain its transfer characteristics.
   (b) Determine the pull-up and pull-down ratio for an nMOS inverter driven by another nMOS inverter.

3. Design a stick diagram for NMOS EX-OR gate.

4. Calculate gate capacitance value of 2 μm technology minimum sized transistor with gate to channel capacitance value of 8×10^4 pF/ohm μm^2.

5. (a) Explain the principle of working of a 4-bit carry-look ahead adder and hence draw the logical schematic used to obtain the generate and propagate signals.
   (b) With the help of the logical schematic explain the working of a parity generator.

6. (a) Summarize the difference between reprogrammable gate array designing and programmable interconnect designing.
   (b) Give a brief description about full custom design. Justify where full custom design is preferred to semicustom design.

7. Compare the simulation process at various levels of design of chips with respect to complexity of computation, speed and accuracy.

8. (a) With the help of schematic diagram using logical blocks explain the working of BILBO as a test pattern generator.
   (b) Discuss about various approaches of design for testability.